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AMENDMENTS TO THE SPECIFICATION

Please replace Abstract with the following rewritten Abstract:

Provided is an adder composed of (N+1) circuit stages in the case of 2.sup.N bits. In the case of N=4 (that is, 16 bits), provisional ~~carriers~~carries that indicate the case where carry is produced from a low order bit and the case where no carry is produced therefrom are generated by conditional cells in a first circuit stage. In second to fourth circuit stages, the provisional ~~carriers~~carries corresponding to higher seven bits other than the most significant bit are converted into provisional sums by converters in a circuit stage in which the provisional ~~carriers~~carries are transferred. In addition, actual carry signals are selected from the provisional ~~carriers~~carries corresponding to lower seven bits other than the least significant bit in a circuit stage in which the provisional ~~carriers~~carries are transferred. In a fifth circuit stage, bit sums for each of the bits are generated and outputted.

Please replace paragraph 0005 of the published application with the following rewritten paragraph:

[0005] FIG. 1 is a circuit diagram showing a 4-bit conditional sum adder of a first conventional example described in, particularly, FIG. 6 in Kuo-Hsing Cheng et al., "The improvement of conditional sum adder for low power applications", 1998. IEEE ASIC Conference Proceedings, pp. 131-134. As shown in FIG. 1, in the first conventional example, when a binary number (A_3, A_2, A_1, A_0) is added to a binary number (B_3, B_2, B_1, B_0), each of conditional cells 111 in a first circuit stage 21 generates both provisional bit sum signals and provisional carry signals and outputs them. Here, the provisional sums include a bit sum signal (for example, S0_1) with respect to the case where carry is produced from a low order bit and a bit sum signal (for

example, S1_1) with respect to the case where no carry is produced. In addition, the provisional ~~carriers~~carries include a carry signal (for example, C0_1) with respect to the case where carry is produced from a low order bit and a carry signal (for example, C1_1) with respect to the case where no carry is produced. In a second circuit stage 22, one of the two provisional sums and one of the two provisional ~~carriers~~carries are selected by multiplexers (MUXs) 120 in accordance with a carry signal from a low order bit and transferred to a next stage. In a third circuit stage 23, actual bit sums S_0 to S_3 and an output carry signal Cout are generated by actual carry signals and outputted to the outside of the adder. According to the first conventional example, because the 2.sup.N-bit adder can be realized by (N+1) circuit stages, the high speed operation is possible. However, in the first conventional example, because the adder includes a large number of multiplexers and the number of wirings is large, power dissipation is large.

Please replace paragraph 0006 of the published application with the following rewritten paragraph:

[0006] As an adder improved to reduce power dissipation, there is a conditional carry adder of a second conventional example described in, particularly, FIG. 7 in Kuo-Hsing Cheng et al., "The improvement of conditional sum adder for low power applications", 1998. IEEE ASIC Conference Proceedings, pp. 131-134. FIG. 2 is a circuit diagram of a 16-bit conditional carry adder. As shown in FIG. 2, in the second conventional example, each of conditional cells 101 (FIG. 4B is a circuit diagram) is different from the conditional cell 111 in the first conventional example. That is, each of the conditional cells 101 in a first circuit stage 31 generates an exclusive OR signal of two input bits (for example, S0_1) and provisional ~~carriers~~carries and outputs them. Here, the provisional ~~carriers~~carries are composed of a pair of signals which are a

carry signal with respect to the case where carry is produced from a low order bit and a carry signal with respect to the case where no carry is produced. In a second circuit stage 32 to a fifth circuit stage 35, each carry signal to be sent to a next circuit stage is selected by a multiplexer (MUX) 120 and a carry selector 110 in accordance with a carry signal from a low order bit and transferred in succession. In a sixth circuit stage 36 including exclusive OR circuits 130, actual bit sums S_1 to S_15 are generated and outputted to the outside of the adder. According to the second conventional example, because only the provisional ~~carriers~~carries may be generated and outputted and no provisional sums are required, the number of multiplexers (one carry selector is counted as two multiplexers) can be reduced. Accordingly, power dissipation at the time of operation can be reduced.

Please replace paragraph 0009 of the published application with the following rewritten paragraph:

[0009] According to the present invention, there is provided a high speed adder in which provisional ~~carriers~~carries composed of a pair of signals that indicate a case where carry is produced from a low order bit and a case where no carry is produced therefrom are generated in advance and an actual ~~carrier~~ carry is selected from the provisional ~~carriers~~carries in accordance with selection information from the low order bit to increase a ~~carrier~~ carry transfer speed, the adder including: a ~~carrier~~ carry transfer path; and a plurality of converters, each of which converts the provisional ~~carriers~~carries into provisional sums composed of a pair of signals that indicate the case where the carry is produced from the low order bit and the case where no carry is produced therefrom, the converters being provided on a predetermined portion of the ~~carrier~~ carry transfer path.

Please replace paragraph 0010 of the published application with the following rewritten paragraph:

[0010] According to the adder of the first conventional example, the provisional ~~carriers~~carries and the provisional sums are generated and transferred in the first circuit stage. In addition, according to the adder of the second conventional example, the provisional ~~carriers~~carries are transferred to generate actual carry signals and all actual bit sums are collectively generated in a final circuit stage. In contrast to these, according to the adder of the present invention, in a circuit stage on the way to the transfer of the ~~carriers~~carries, the provisional ~~carriers~~carries are converted into the provisional sums and transported. According to the structure of the adder of the present invention, the number of multiplexers and the number of input and output wirings for the multiplexers can be reduced as compared with the adder of the first conventional example. In addition, the adder can be realized by the number of circuit stages smaller than that in the second conventional example.

Please replace paragraph 0023 of the published application with the following rewritten paragraph:

[0023] FIG. 3 is a circuit diagram showing a 16-bit adder according to an embodiment of an adder of the present invention. In the adder shown in FIG. 3, as in the case of the second conventional example shown in FIG. 2, 16-bit input data (A_15 to A_0) and (B_15 to B_0) and an input carry signal Cin are inputted thereto and 16-bit sum output signals (S_15 to S_0) indicating the sums thereof and an output carry signal Cout are outputted therefrom. However, the adder shown in FIG. 3 is distinguished from the second conventional example by the following points. That is, the exclusive OR circuits that output actual bit sums S_1 to S_8 in the

circuit stage 36 shown in FIG. 2 is included in a final stage, and, the exclusive OR circuits that output the actual bit sums S_9 to S_15 are replaced by each of converters 140 in which provisional ~~carriers~~carries composed of a pair of carry signals are inputted and converted into provisional sums composed of a pair of bit sum signals and the provisional sums are outputted.

Please replace paragraph 0025 of the published application with the following rewritten paragraph:

[0025] In a 2.sup.N-bit adder to which the present invention is applied, a first circuit stage includes (2.sup.N-1) conditional cells 101 and a full adder 100. Each of the conditional cells 101 is provided corresponding to the most significant bit to a bit larger than the least significant bit by one bit, performs exclusive OR calculation on corresponding bits of two input data which are inputted thereto, generates provisional ~~carriers~~carries composed of a pair of signals that indicate the case where carry is produced from a low order bit and the case where no carry is produced, and outputs the provisional ~~carriers~~carries. The full adder 100 generates an exclusive OR signal and a carry signal in accordance with the least significant bits of the two input data and an input carry signal, which are inputted thereto. The function of each of the conditional cells 101 and the function of the full adder 100 are the same as in the second conventional example.

Please replace paragraph 0026 of the published application with the following rewritten paragraph:

[0026] FIG. 4A shows an internal structure of a first circuit stage 11 in the 16-bit adder shown in FIG. 3. The two input data are inputted to 15 (=2.sup.4-1) conditional cells 101 and the full adder. Each of the conditional cells 101 is provided for each bit of the same digit from the most

significant bit in the low order direction. The full adder is provided corresponding to the least significant bit. Each of the conditional cells 101 generates an exclusive OR signal of inputted two bits (for example, S0_1). In addition, each of the conditional cells 101 generates a carry signal (for example, C0_1) in the case where it is assumed that an input carry signal from a low order bit is 0 (that is, no carry is produced) and a carry signal (for example, C1_1) in the case where it is assumed that the input carry signal from the low order bit is 1 (that is, carry is produced) and outputs the carry signals as provisional ~~carriers~~carries composed of a pair of signals. Accordingly, exclusive OR signals S0_1 to S0_15, carry signals (C0_1 to C0_15) in the case where it is assumed that no carry is produced from the low order bit, and carry signals (C1_1 to C1_15) in the case where it is assumed that carry is produced from the low order bit are outputted from the first circuit stage. The full adder 100 is used for the least significant bits. Bits A_0 and B_0 and an input carry signal Cin are simultaneously inputted to the full adder 100 and an actual bit sum S_0 and an actual carry signal Cout_0 are outputted therefrom.

Please replace paragraph 0030 of the published application with the following rewritten paragraph:

[0030] In the case of such division, one multiplexer (MUX) 120 is provided corresponding to higher 2.sup.(N-M-1) (=1) bits in the sub-circuit P2.sub.1 which is a first sub-arithmetic circuit, including inputs from 2.sup.(N-M)-th (=second) bits from the least significant bits A_0 and B_0 in the high order direction. The pair of signals C0_1 and C1_1 which are the outputs of the conditional cells 101 provided for corresponding bits in the first circuit stage 11 which is the preceding circuit stage and indicate the provisional ~~carriers~~carries are inputted to the multiplexer. With respect to the multiplexer, a carry signal Cout_0 which is outputted from the full adder 100

provided for bits in the first circuit stage 11, which correspond to (2.sup.(N-M-1)+1)-th (=second) bits from the high order in the sub-circuit P2.sub.1 is inputted there to as a selection signal. The multiplexer outputs a signal 300, which is an actual carry signal in accordance with the carry signal Cout_0.

Please replace paragraph 0031 of the published application with the following rewritten paragraph:

[0031] Also, the (2.sup.(N-1)-2.sup.(N-M-1)) (=7) carry selectors 110 are provided corresponding to higher 2.sup.(N-M-1) (=1) bit in the sub-circuit P2.sub.8 corresponding to a second sub-arithmetic circuit to which the signals C0_15 and C1_15 as the carry signals corresponding to the most significant bits A_15 and B_15 are inputted and in the corresponding sub-circuits of a third sub-arithmetic circuit including sub-circuits corresponding to the second sub-circuit P2.sub.7and the second ((=2.sup.M-1)-th) (=seventh) sub-circuit P2.sub.2 counted down from the sub-circuit P2.sub.8. The pair of signals which are outputs of the conditional cells which are provided for the corresponding bits in the first circuit stage 11 that is the preceding circuit stage are inputted to each of the carry selectors. In addition, the pair of selection signals which are the outputs of the conditional cells 101 provided for the bits in the first circuit stage 11, which correspond to (2.sup.(N-M-1)+1)th (=second) bits from the higher bits in the sub-circuit are inputted to each of the carry selectors. Each of the carry selectors in the second sub-arithmetic circuit (P2.sub.8) and the third sub-arithmetic circuit (P2.sub.2 to P2.sub.7) selects a pair of signal indicating provisional ~~carrierscarries~~ or the provisional sums in the following circuit stage in accordance with the selection signals and outputs the selected signals.

Please replace paragraph 0033 of the published application with the following rewritten paragraph:

[0033] Also, the converter 140 is provided corresponding to a lower 2.sup.(N-M-1) (=1) bit in the sub-circuit P2.sub.8 which is the second sub-arithmetic circuit. The pair of signals C0_14 and C1_14 and the exclusive OR signal S0_15 are inputted to the converter. The pair of signals C0_14 and C1_14 are the outputs of the conditional cell 101 provided for corresponding bits in the first circuit stage 11 which is the preceding circuit stage and indicate the provisional ~~carriers~~carries. The exclusive OR signal S0_15 is outputted from the conditional cell corresponding to the bit higher by one bit in the first circuit stage 11. Then, the converter converts the inputted signals into a pair of signals 313 and 314 indicating the provisional sums and outputs the converted signals.

Please replace paragraph 0036 of the published application with the following rewritten paragraph:

[0036] The converter 140 will be described by using a converter included in the sub-circuit P2.sub.8 as shown in FIG. 5 as an example. The converter 140 is composed of a first exclusive OR circuit and a second exclusive OR circuit. When the signal C0_14 which is one of the pair of signals C0_14 and C1_14 indicating the provisional ~~carriers~~carries and the exclusive OR signal S0_15 outputted from the conditional cell corresponding to the bit higher by one bit in the first circuit stage 11 are inputted, the first exclusive OR circuit outputs the signal 313 which is one of the pair of signals 313 and 314 indicating the provisional sums. When the signal C1_14 which is the other of the pair of signals C0_14 and C1_14 and the exclusive OR signal S0_15 are

inputted, the second exclusive OR circuit outputs the signal 314 which is the other of the pair of signals 313 and 314 indicating the provisional sums.

Please replace paragraph 0038 of the published application with the following rewritten paragraph:

[0038] In the case of such division, two multiplexers 120 are provided corresponding to high 2.sup.(N-M-1) (=2) bits in the sub-circuit P3.sub.1 which is a first sub-arithmetic circuit, including inputs from 2.sup.(N-M)-th (=fourth) bits from the least significant bits A_0 and B_0 in the high order direction. The pair of signals 301 and 302 which are the outputs of the carry selector 110 provided for corresponding bits in the second circuit stage 12 which is the preceding circuit stage and indicate the provisional ~~carriers~~carries are inputted to the multiplexer provided corresponding to the high order bit. In addition, the pair of signals C0_2 and C1_2 which are the outputs of the conditional cell 101 provided for corresponding bits in the first circuit stage 11 which is the preceding circuit stage and indicate the provisional ~~carriers~~carries are inputted to the multiplexer provided corresponding to the low order bit. With respect to these multiplexers, the signal 300 which is outputted from the multiplexer 120 provided for bits in the circuit stage 12, which correspond to (2.sup.(N-M-1)+1)-th (=third) bits from the high order in the sub-circuit P3.sub.1 is inputted thereto as a selection signal. The multiplexer provided corresponding to the high order bit outputs a signal 401, which is an actual carry signal in accordance with the signal 300. In addition, the multiplexer provided corresponding to the low order bit outputs a signal 400, which is an actual carry signal in accordance with the signal 300.

Please replace paragraph 0039 of the published application with the following rewritten paragraph:

[0039] Also, the (2.sup.(N-1)-2.sup.(N-M-1)) (=6) carry selectors 110 are provided corresponding to each high 2.sup.(N-M-1) (=2) bits in the sub-circuit P3.sub.4 corresponding to a second sub-arithmetic circuit to which the signals 315 and 316 as the provisional carry signals corresponding to the most significant bits A_15 and B_15 are inputted and in the corresponding sub-circuits of a third sub-arithmetic circuit including sub-circuits corresponding to the second sub-circuit P3.sub.3 and the third ((=2.sup.M-1)-th)) sub-circuit P3.sub.2 from the sub-circuit P3.sub.4 in the low order direction. The pair of signals from any one of the conditional cell 101, the carry selector 110, and the converter 140, which are provided for the corresponding bits in the preceding circuit stages are inputted to each of the carry selectors. In addition, the pair of selection signals which are the outputs of the carry selector 110 provided for the bits in the second circuit stage 12, which correspond to (2.sup.(N-M-1)+1)-th (=third) bits from the high order in the sub-circuit are inputted to each of the carry selectors. Each of the carry selectors in the second sub-arithmetic circuit (P3.sub.4) and the third sub-arithmetic circuit (P3.sub.2 to P3.sub.3) selects a pair of signals indicating provisional ~~carriers~~carries or the provisional sums in the following circuit stage in accordance with the selection signals and outputs the selected signals.

Please replace paragraph 0041 of the published application with the following rewritten paragraph:

[0041] Also, the two converters 140 are provided corresponding to lower 2.sup.(N-M-1) (=2) bits in the sub-circuit P3.sub.4 which is the second sub-arithmetic circuit. The pair of signals 311 and

312 and the exclusive OR signal S0_14 are inputted to the first converter from the top, of the two converters 140. The pair of signals 311 and 312 are the outputs of the carry selector 110 provided for corresponding bits in the second circuit stage 12 which is the preceding circuit stage and indicate the provisional ~~carriers~~carries. The exclusive OR signal S0_14 is outputted from the conditional cell corresponding to the bit higher by one bit in the first circuit stage 11. Then, the first converter from the top converts the inputted signals into a pair of signals 412 and 413 indicating the provisional sums and outputs the converted signals. The pair of signals C0_12 and C1_12 and the exclusive OR signal S0_13 are inputted to second converter from the top, of the two converters 140. The pair of signals C0_12 and C1_12 are the outputs of the carry selector 110 provided for corresponding bits in the first circuit stage 11 which is the preceding circuit stage and indicate the provisional ~~carriers~~carries. The exclusive OR signal S0_13 is outputted from the conditional cell corresponding to the bit higher by one bit in the first circuit stage 11. Then, the second converter from the top converts the inputted signals into a pair of signals 410 and 411 indicating the provisional sums and outputs the converted signals.

Please replace paragraph 0043 of the published application with the following rewritten paragraph:

[0043] In the case of such division, four multiplexers 120 are provided corresponding to high 2.sup.(N-M-1) (=4) bits in the sub-circuit P4.sub.1 which is a first sub-arithmetic circuit, including inputs from 2.sup.(N-M)-th (=eighth) bits from the least significant bits A_0 and B_0 in the high order direction. The pair of signals 404 and 405 which are the outputs of the carry selector 110 provided for corresponding bits in the third circuit stage 13 which is the preceding circuit stage, and which indicate the provisional ~~carriers~~carries are inputted to the first

multiplexer from the top. The signal 401, which is outputted from the multiplexer 120 provided for the bits in the third circuit stage 13, which correspond to (2.sup.(N-M-1)+1)-th (=fifth) bits from the high order in the sub-circuit P4.sub.1, is used as a selection signal. Then, the first multiplexer from the top selects an actual carry signal in accordance with the selection signal and outputs a signal 503. The pair of signals 402 and 403 which are the outputs of the carry selector 110 provided for corresponding bits in the third circuit stage 13 which is the preceding circuit stage, and which indicate the provisional ~~carriers~~carries are inputted to the second multiplexer from the top. The signal 401 is used as the selection signal. Then, the second multiplexer from the top selects an actual carry signal in accordance with the selection signal and outputs a signal 502. The pair of signals 303 and 304 which are the outputs of the carry selector 110 provided for corresponding bits in the second circuit stage 12 which is the preceding circuit stage, and which indicate the provisional ~~carriers~~carries are inputted to the third multiplexer from the top. The signal 401 is used as the selection signal. Then, the third multiplexer from the top selects an actual carry signal in accordance with the selection signal and outputs a signal 501. The pair of signals C0_4 and C1_4 which are the outputs of the conditional cell 101 provided for corresponding bits in the first circuit stage 11 which is the preceding circuit stage, and which indicate the provisional ~~carriers~~carries are inputted to the fourth multiplexer from the top. The signal 401 is used as the selection signal. Then, the fourth multiplexer from the top selects an actual carry signal in accordance with the selection signal and outputs a signal 500.

Please replace paragraph 0044 of the published application with the following rewritten paragraph:

[0044] Also, the (2.sup.(N-1)-2.sup.(N-M-1)) (=4) carry selectors 110 are provided corresponding to high 2.sup.(N-M-1) (=4) bits in the sub-circuit P4.sup.2 corresponding to a second sub-arithmetic circuit to which the signals 416 and 417 as the carry signals corresponding to the most significant bits A_15 and B_15 are inputted. The pair of signals outputted from any one of the conditional cell 101, the carry selector 110, and the converter 140, which are provided for the corresponding bits in the preceding circuit stages are inputted to each of the carry selectors. In addition, the pair of selection signals which are outputted from the carry selector 110 provided for the bits in the third circuit stage 13, which correspond to (2.sup.(N-M-1)+1)-th (=fifth) bits from the high order in the sub-circuit P4.sub.2 are inputted to each of the carry selectors. Each of the carry selectors selects a pair of signal indicating provisional ~~carriers~~carries or the provisional sums in the following circuit stage in accordance with the selection signals and outputs the selected signals.

Please replace paragraph 0045 of the published application with the following rewritten paragraph:

[0045] In other words, the pair of signals 416 and 417 which are the outputs of the carry selector in the third circuit stage 13 are inputted to the first carry selector from the top, of the four carry selectors 110 included in the sub-circuit P4.sub.2. Then, the first carry selector from the top performs selection in accordance with the pair of selection signals 408 and 409 which are the outputs of the carry selector in the third circuit stage 13, which is provided for the bits corresponding to (2.sup.(N-M-1)+1)-th (=fifth) bits from the high order in the sub-circuit

P4.sub.2 and outputs a pair of signals 518 and 519. Similarly, the pair of signals 414 and 415 which are the outputs of the carry selector in the third circuit stage 13 are inputted to the second carry selector from the top. Then, the second carry selector from the top performs selection in accordance with the pair of selection signals 408 and 409 and outputs a pair of signals 516 and 517. In addition, the pair of signals 412 and 413 which are the outputs of the carry selector in the third circuit stage 13 are inputted to the third carry selector from the top. Then, the third carry selector from the top performs selection in accordance with the pair of selection signals 408 and 409 and outputs a pair of signals 514 and 515. In addition, the pair of signals 410 and 411 which are the outputs of the carry selector in the third circuit stage 13 are inputted to the lowest order ~~carrier~~ carry selector, that is, the fourth carry selector from the top. Then, the fourth carry selector from the top performs selection in accordance with the pair of selection signals 408 and 409 and outputs a pair of signals 512 and 513.

Please replace paragraph 0046 of the published application with the following rewritten paragraph:

[0046] Also, the four converters 140 are provided corresponding to low 2.sup.(N-M-1) (=4) bits in the sub-circuit P4.sub.2 which is the second sub-arithmetic circuit. The pair of signals 408 and 409 and the exclusive OR signal S0_12 are inputted to the first converter from the top, of the four converters 140. The pair of signals 408 and 409 are the outputs of the carry selector 110 provided for corresponding bits in the third circuit stage 13 which is the preceding circuit stage and indicate the provisional ~~carriers~~carries. The exclusive OR signal S0_12 is outputted from the conditional cell corresponding to the bit higher by one bit in the first circuit stage 11. Then, the first converter from the top converts the inputted signals into a pair of signals 510 and 511

indicating the provisional sums and outputs the converted signals. Similarly, the pair of signals 406 and 407 and the exclusive OR signal S0_11 are inputted to the second converter from the top. The pair of signals 406 and 407 are the outputs of the carry selector 110 provided for corresponding bits in the third circuit stage 13 which is the preceding circuit stage and indicate the provisional ~~carriers~~carries. The exclusive OR signal S0_11 is outputted from the conditional cell corresponding to the bit higher by one bit in the first circuit stage 11. Then, the second converter from the top converts the inputted signals into a pair of signals 508 and 509 indicating the provisional sums and outputs the converted signals. In addition, the pair of signals 307 and 308 and the exclusive OR signal S0_10 are inputted to the third converter from the top. The pair of signals 307 and 308 are the outputs of the carry selector 110 provided for corresponding bits in the second circuit stage 12 which is the preceding circuit stage and indicate the provisional ~~carriers~~carries. The exclusive OR signal S0_10 is outputted from the conditional cell corresponding to the bit higher by one bit in the first circuit stage 11. Then, the third converter from the top converts the inputted signals into a pair of signals 506 and 507 indicating the provisional sums and outputs the converted signals. In addition, the pair of signals C0_8 and C1_8 and the exclusive OR signal S0_9 are inputted to the lowest order converter, that is, the fourth converter from the top. The pair of signals C0_8 and C1_8 are the outputs of the conditional cell 101 provided for corresponding bits in the first circuit stage 11 which is the preceding circuit stage and indicate the provisional ~~carriers~~carries. The exclusive OR signal S0_9 is outputted from the conditional cell corresponding to the bit higher by one bit in the first circuit stage 11. Then, the fourth converter from the top converts the inputted signals into a pair of signals 504 and 505 indicating the provisional sums and outputs the converted signals.

Please replace paragraph 0053 of the published application with the following rewritten paragraph:

[0053] Next, in the second circuit stage 12, the provisional carry signals generated in each of the bits are divided corresponding to the sub-circuits P2.sub.1 to P2.sub.8 for every two bits. Each of the sub-circuits P2.sub.1 to P2.sub.8 generates new provisional ~~carriers~~carries selected in accordance with the provisional ~~carriers~~carries from the bit lower by one bit and outputs the new provisional ~~carriers~~carries. The selection of the provisional ~~carriers~~carries is performed by the carry selector 110 shown in FIG. 6B. The provisional ~~carriers~~carries from the bit lower by one bit, which are inputted as the selection signals to each of the carry selectors in the second circuit stage 12 are generated while assuming the case where carry is produced from the bit further lower by one bit and the case where no carry is produced therefrom. Accordingly, the provisional carry signal outputted from a Cout1 terminal of each of the carry selectors in the second circuit stage 12 is generated while assuming the case where carry is produced from the bit lower by two bits. In addition, the provisional carry signal outputted from a Cout0 terminal of each of the carry selectors is generated while assuming the case where no carry is produced from the bit lower by two bits. That is, because the carry signal Cout_0 of the least significant bit is the actual carry signal, the multiplexer corresponding to the second bit from the least significant bit (that is, the multiplexer 120 in the sub-circuit P2.sub.1) selects the actual carry signal 300 from the pair of signals C0_1 and C1_1 indicating the provisional ~~carriers~~carries and outputs the actual carry signal 300.

Please replace paragraph 0055 of the published application with the following rewritten paragraph:

[0055] Next, in FIG. 7 that shows the third circuit stage 13 shown in FIG. 3, the provisional ~~carriers~~carries and the provisional sums which are inputted thereto are divided corresponding to the sub-circuits P3.sub.1 to P3.sub.4 for every four bits. In the k(k is 2, 3, or 4)-th sub-circuit P3.sub.k, the provisional ~~carriers~~carries composed of the pair of signals generated in the high two bits are selected in accordance with the provisional ~~carriers~~carries from the third bit from the most significant bit in the sub-circuit P3.sub.k, so that new provisional ~~carriers~~carries are generated and outputted. Here, the provisional ~~carriers~~carries used as the selection signals are generated while assuming the presence or absence of carry from the most significant bit in the sub-circuit P3.sub.k-1 lower by one order. Therefore, the provisional ~~carriers~~carries and the provisional sums which are newly generated in the sub-circuit P3.sub.k and outputted there from are all generated while assuming the presence or absence of carry from the most significant bit in the sub-circuit P3.sub.k-1 lower by one order. In the lowest order sub-circuit P3.sub.1, the signal 300 corresponding to the third bit from the most significant bit is the actual carry signal. Therefore, the signals 401 and 400 which are selected using the signal 300 as the selection signal by the two multiplexers included in the sub-circuit P3.sub.1 and outputted therefrom are the actual carry signals.

Please replace paragraph 0057 of the published application with the following rewritten paragraph:

[0057] Next, in FIG. 8 that shows the fourth circuit stage 14, the provisional ~~carriers~~carries and the provisional sums which are inputted thereto are divided corresponding to the sub-circuits

P4.sub.1 and P4.sub.2 for every eight bits. In the sub-circuit P4.sub.2, the provisional ~~carriers~~carries and the provisional sums which are composed of the pair of signals generated in the high four bits are selected in accordance with the provisional ~~carriers~~carries 408 and 409 from the fifth bit from the most significant bit in the sub-circuit P4.sub.2, so that new provisional ~~carriers~~carries and new provisional sums are generated and outputted. Here, the pair of provisional carry signals 408 and 409 used as the selection signals are generated while assuming the presence or absence of carry from the most significant bit in the sub-circuit P4.sub.1 lower by one order. Therefore, the provisional ~~carriers~~carries and the provisional sums which are newly generated in the sub-circuit P4.sub.2 and outputted therefrom are all generated while assuming the presence or absence of carry from the most significant bit in the sub-circuit P4.sub.1 lower by one order. In the low order sub-circuit P4.sub.1, the signal 401 corresponding to the fifth bit from the most significant bit is the actual carry signal. Therefore, all the signals 503, 502, 501, and 500 which are selected using the signal 401 as the selection signal by the four multiplexers included in the sub-circuit P4.sub.1 and outputted therefrom are the actual carry signals.

Please replace paragraph 0059 of the published application with the following rewritten paragraph:

[0059] Next, in FIG. 9 that shows the fifth circuit stage 15 which is the final stage as shown in FIG. 3, the provisional sums are inputted to seven multiplexers (second to eighth multiplexers from the top) of the multiplexers provided corresponding to eight bits from the most significant bit. The seven multiplexers perform selection in accordance with the actual carry signal 503 from the ninth bit from the most significant bit and output the signals S_15 to S_9 which are the actual bit sum signals to the outside of the adder. The multiplexer corresponding to the most significant

bit selects one of the pair of signals 519 and 518 indicating the provisional ~~carriers~~carries in accordance with the signal 503 and outputs the output carry signal Cout as a carry signal generated by adding the two input data to the outside of the adder. With respect to the ninth to sixteenth bits from the most significant bit, the actual carry signals are determined after the operation of the fourth circuit stage 14. Accordingly, as shown in FIG. 9, the eight exclusive OR circuits generate the actual bit sums S_8 to S_1 by exclusive OR operation between the actual carry signals and the bit sum signal S0_8 to S0_1 generated in the first circuit stage 11, and output the generated actual bit sums S_8 to S_1 to the outside of the adder. The signal S_0 generated in the first circuit stage 11 is outputted as the actual bit sum of the least significant bit to the outside of the adder without processing.

Please replace paragraph 0060 of the published application with the following rewritten paragraph:

[0060] According to the adder of the first conventional example as shown in FIG. 1, the ~~carriers~~carries and the sums are generated in the first circuit stage and transferred. In addition, according to the adder of the second conventional example as shown in FIG. 2, the ~~carriers~~carries are transferred to generate the actual carry signals and all actual bit sums are generated in the final circuit stage at once. In contrast to those, according to the adder of the present invention, the provisional ~~carriers~~carries are converted into the provisional sums in a circuit stage in which the ~~carriers~~carries are transferred. Accordingly, according to the adder of the present invention, the number of multiplexers and the number of input and output wirings for the multiplexers can be reduced as compared with the adder of the first conventional example in which the ~~carriers~~carries and the sums are generated for all bits and transferred. Thus, power

dissipation can be reduced. In addition, the adder of the present invention can be realized by the number of circuit stages equal to that in the first conventional example (that is, the number of circuit stages smaller than that in the second conventional example by one) Thus, as compared with the adder of the second conventional example, it is possible that adding is executed at high speed.

Please replace paragraph 0062 of the published application with the following rewritten paragraph:

[0062] Also, the number of circuit stages necessary to construct the adder of the second conventional example is compared with the number of circuit stages necessary to construct the adder of the present invention. In the case where the 16-bit adder is constructed, although 6 circuit stages are required for the adder of the second conventional example, the adder of the present invention can be constructed by 5 circuit stages. In the case of the 32-bit adder, although 7 circuit stages are required for the adder of the second conventional example, the adder of the present invention can be constructed by 6 circuit stages. Thus, the number of logic stages in a critical path of the adder of the present invention can be reduced by one as compared with that of the adder of the second conventional example, and the adder of the present invention can be realized by the number of logic stages equal to that in the adder of the first conventional example. Here, the number of logic stages indicates the sum total of the numbers of conditional cells, multiplexers, carry selectors, converters, and exclusive OR circuits, which are located on a path on which the ~~carriers~~carries or the sums are transferred from the first circuit stage to the final circuit stage.